REMARKS

Claims 1-19 are all the claims presently pending in the application. New claims 13-19 have been added to claim additional features of the invention.

It is noted that the claim amendments are made only for more particularly pointing out the invention, and not for distinguishing the invention over the prior art, narrowing the claims or for any statutory requirements of patentability. Further, Applicant specifically states that no amendment to any claim herein should be construed as a disclaimer of any interest in or right to an equivalent of any element or feature of the amended claim.

Claims 1-12 stand rejected under 35 USC §102(e) as allegedly anticipated by US Patent 6,782,354 to Ikegami.

This rejection is respectfully traversed in the following discussion.

I. THE CLAIMED INVENTION

As described and as defined in, for example, claim 1, the claimed invention is directed to an apparatus for estimating power consumption. A behavioral synthesis unit to which an algorithm-level description is input converts the algorithm-level description to a clock-based description and behavioral synthesis information. A clock-based simulation unit to which the clock-based description and behavioral synthesis information are input executes a clock-based simulation and calculates a power consumption factor of a storage element based upon both the clock-based description and behavioral synthesis information.

Conventional methods, as described beginning at line 12 on page 1, can be broken down into either an RTL HDL simulation or a clock-based simulation. The clock-based description has a lower level of abstraction than the algorithmic language and a higher level of abstraction than the RTL HDL. However, as stated at lines 6-8 of page 10, the RTL HDL simulation is much slower than clock-based simulation.

The claimed invention, on the other hand, provides a method wherein both a clock-based description and behavioral synthesis information is provided to a clock-based simulation for storage elements. The behavioral synthesis information allows a different clock-based simulation for different types of storage elements, since the memory element can be either based on registers or on a memory array.

II. THE PRIOR ART REJECTION

The Examiner alleges that Ikegami teaches the claimed invention defined by claims 1-12. Applicant submits, however, that there is at least one elements of the claimed invention which are neither taught nor suggested by Ikegami.

That is, although Ikegami arguably discloses a clock-based simulation method, its method is based upon an assumption that the memory devices are registers, as clearly evident from noting that the VHDL description beginning at line 18 of column 12 contains only a subroutine for a register (e.g., "RT hardware description 12" at lines 52 of column 14), but no subroutine for a memory array that could alternatively provide a function as a memory storage device.

Therefore, Applicants submit that, whatever similarities there might be between Ikegami and the present invention, there is no teaching or suggestion in Ikegami that the memory units be anything other than registers. Indeed, a key feature of Ikegami is the ability to determine how the limited number of registers can be shared, as explained at lines 48-50 of column 6.

Thus, because it presumes that all relevant storage units will be registers, there is no need in Ikegami to provide an additional input that describes the type of storage unit to be simulated.

That is, there is no need in Ikegami to provide a behavioral synthesis information to describe the type of storage unit to be simulated. Indeed, because of its presumption that the storage units will be registers, Applicants submit that Ikegami clearly teaches against providing this additional input into the clock-based simulation.

Hence, turning to the clear language of the claims, in Ikegami there is no teaching or suggestion of: "...a behavioral synthesis unit to which an algorithm-level description is input for converting the algorithm-level description to a clock-based description and behavioral synthesis information; and a clock-based simulation unit to which the clock-based description and behavioral synthesis information are input for executing a clock-based simulation and calculating a power consumption factor of a storage element based upon both the clock-based description and behavioral synthesis information."

Moreover, relative to the rejection for claims 2 and 8, Applicants submit that the locations in Ikegami to which the Examiner points do not provide any indication whatsoever that different types of alternative storage elements are available for simulation by the clock-based simulation. All of the descriptions in Ikegami presume that the storage elements are registers.

Relative to the rejection for the remaining dependent claims 3-6 and 9-12, Applicants submit that the terminology "toggle-rate and/or transition probability" include terms of art. The clock simulation of Ikegami is not at all described as corresponding to a technique that uses "toggle-rate" or "transition probability", since it clearly merely uses a progressive clock signal, as evident from the description of the four cases, beginning at line 66 of column 11.

This clocking technique is different from the toggle rate and transition probability technique described beginning at lines 15 in the disclosure of the present invention.

Therefore, Applicants submit that the rejection currently of record for claims 3-6 and 9-12 fails to meet the initial burden of a *prima facie* rejection, since the plain meaning of the claim language has not been heeded.

Therefore, Applicant submits that there are elements of the claimed invention that are not taught or suggest by Ikegami. Therefore, the Examiner is respectfully requested to reconsider and withdraw this rejection based on Ikegami.

III. FORMAL MATTERS AND CONCLUSION

Further, the Examiner is again requested to consider the reference (e.g., JP-P2001-109788A) submitted in the IDS of July 22, 2003. It is noted that the IDS was in full compliance with M.P.E.P. § 609 AND 37 C.F.R. § 1.98. It is noted that a concise statement of relevance for the reference is found at page 2 of the present application, beginning at line 15. For the Examiner's convenience, another PTO-1449 form is attached hereto for the Examiner's consideration and initials.

In view of the foregoing, Applicant submits that claims 1-19, all the claims presently pending in the application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Attorney's Deposit Account No. 50-0481.

Respectfully Submitted,

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